Dynamic CMOS Logic using clock gating in Deep Submicron Technology

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Abstract: The use of dynamic logic CMOS circuits for optimizes design constraints of speed and area requirements, are making signal integrity one of the most critical metrics of performance. Noise can have adverse effects on functional correctness, power, timing, and reliability of CMOS digital circuits. The number of problem arises in this structure firstly, the inputs can only change during the precharge phase and must be stable during the evaluate portion of the cycle. If this condition is not met, charge redistribution effects can corrupt the output node voltage. This paper discusses the behavior of CMOS dynamic logic circuit and sources of noise in these circuits. Output variation caused by noise can results in performance disturbance in digital integrated circuits.

Keywords: Dynamic CMOS, Domino Logic, Precharge, Evaluate logic

I. Introduction:

Dynamic CMOS logic circuit is the better style of design for optimize speed, area and improved performance computing. The switching and propagation delay is improved by using dynamic logic by the use of NMOS transistor in pull down network (PDN) of circuit. But dynamic logic has an imperative design challenge of noise tolerance, charge leakage and power dissipation. The CMOS circuit performance is possible to improve by reducing the supply voltage, technology scaling in device size and dimensions, MOSFET threshold voltage form many years. But these may cause the increase in leakage power dissipations in the circuit. This power dissipation are cause mainly due to switching activities of the circuit at output load capacitors called as dynamic power dissipation while the power dissipation due to the parasitic leakage components in the CMOS circuit called as static power dissipation. Thus there is need for reducing the power dissipation in deep submicron technology.

II. Overview of Previous Works

A many design techniques have been propose in the previous years to reduce power dissipation in dynamic logic circuits, feedback keepers were proposed to prevent the dynamic node precharged to remove the charge sharing problem and weak complementary p-network is constructed to develop the noise susceptible CMOS logic gates. On the other hand, the techniques to improve dynamic circuit noise susceptible at a considerable cost in terms of one or more other significant design constraints like area, speed, and power consumption. A clock gating with output hold circuitry is design in [1]. A Clock signal is connected to the domino logic when it is in the active state. For the duration of static mode, clock is bypass when the state of the circuit is retained. A 2X1 Mux is propose using clock gating and for retaining the state of the circuit. Timing Simulation analysis is carried out in a NAND logic gate, NOR logic gate and 1-bit full adder unit in 16nano meter technology. The power dissipation of the domino logic circuit is decreases up to an average of 99.37 percent w.r.t standard domino logic. The path Propagation delay is somewhat increased to an average of 4.53%. Area of the proposed circuit enhance to four transistors in each CMOS domino logic circuit [1]. The effect of process variation on delay is analyzed in depth for both static and dynamic CMOS logic styles in [3]. Analysis allows for gaining an insight into the delay dependence on fan-in, fan-out, and sizing in sub-100-nm technologies. Simple but reasonably accurate models are derived to capture the basic dependences. The effect of process variations in transistor stacks is analytically modeled and analyzed in detail [3][2]. The path propagation delay in dynamic logic is dependent on the number and width of transistor [4]. The variation (reduce) in size of the transistor will also vary (reduce) the discharging current and also vary the output pull down path delay. Increasing width of transistors to reduce one path delay may increase the capacitive load of channel connected transistors on other paths and, substantially increase their delays. his complexity increases along with the number of paths present in the circuit. Implemented using 90- nm CMOS process, the proposed algorithm has demonstrated an average improvement in worst-

case delay by 34%, delay uncertainty by 40.3%, delay sensitivity by 25.1%, and noise margins by 19.4% when compared to their initial performances [4].

III. Noise in Dynamic Design:

The dynamic circuit concept results in simple and fast structure at the expense of a reduced robustness with regards to noise. The logic has a number of deficiencies that must be dealt with to guarantee functional operation.

Charge leakage:

The operation of the dynamic logic depends on the principles of dynamically storing a charge on the output node (capacitor). Due to leakage currents, this charge gradually leaks away, resulting eventually in malfunctioning of the gate.

Charge sharing:

During the precharge phase, the output node is precharged to VDD. Node Capacitors represent the parasitic capacitances of the internal nodes of the circuit share the charge. This causes a drop in the output voltage, which cannot be recovered due to the dynamic nature of the circuit. Charge sharing between the dynamic node and the internal nodes in the pull-down network often results in false gate switching. A simple yet effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull down network along with precharging the dynamic node.

Clock feed through:

The clock signal is coupled to the storage node by the gate-source capacitance and the gate-overlap capacitance of the precharge device. The fast rising and falling edges of the clock couple into the signal node. The danger of clock feed-through is that it causes the signal level to rise sufficiently above the supply voltage as to forward-bias the junction diode. This causes electron injection into the substrate and eventually resulting in faulty operation

Input noise: It refers to noise presented at the inputs of a logic gate. They are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. To improve noise tolerance against both internal and external noises is to increase the source voltage of the transistors in the pull-down network.

Power and ground noise: It is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package. Power and ground networks can also be contaminated by external noises from chip pins.

Substrate noise: It can affect the signal integrity of a logic gate through substrate coupling.

IV. Dynamic Verses Static CMOS Logic:

In static CMOS circuit the charging and discharging path from power or ground to the output node capacitor is controlled by input signals through pull up (design by PMOS) and pull down networks (design by NMOS). Out of these two nretwork only one network operate at a time i.e these networks are designed such that the pull up and pull down networks are never ‘on’ simultaneously. Whereas dynamic CMOS circuit is design with percharge and evaluate logic. Here the precharage transistor is use instead of pull up network in static CMOS and the evaluate transistor is connected between the pull down network design and ground supply rail. This logic requires less number of transistors thus dynamic logic is good choice for its advantages of low area and high speed due to lower capacitance and absence of contention during switching.

V. Dynamic MOS Logic:

The CMOS Dynamic logic operates in two phases; these are precharge phase and evaluation phase. Dynamic logic is a clocked logic family which means that there is a clock in every logic gate. The continuous switching of clock in domino logic design leads to the higher power dissipation. A typical n-type dynamic CMOS NAND logic gate, as shown in Fig. 1, consists of clock controlled transistors MOS1 and MOS2, a pull-down n-type transistor network, and an output driver

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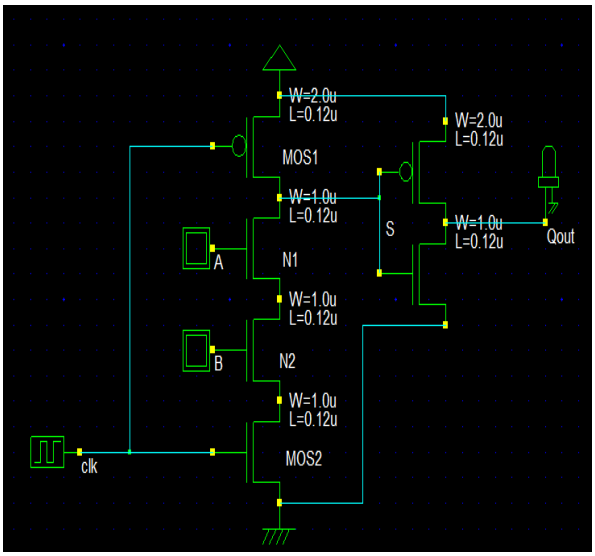

Fig1 : Dynamic CMOS NAND Logic

Fig1 shows the dynamic CMOS logic for precharge and evaluate base NAND logic gate. A common clock (clk) is connected to the precharge PMOS and evaluates NMOS transistors. The output node value is evaluate as per the input

value input port A and B. The output driver inverter is connected across the output node of precharge and evaluates logic circuit.

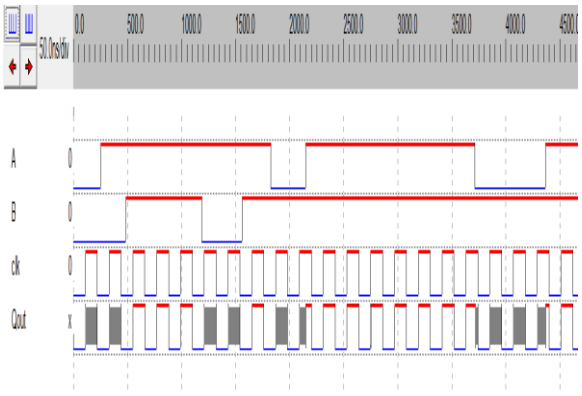

Fig 2: Timing Wave of Dynamic CMOS NAND Logic

The operation of a dynamic CMOS NAND logic gate can be divided into two phases. In the precharge phase when the clock clk is low, the dynamic node S is charged to logic high through MOS1 and the output of the gate Q is low. The evaluation phase starts when the clock goes high. In this phase, MOS1 is OFF and MOS2 is ON. The dynamic node S discharges or retains its charge depending on the inputs to the pull-down network. The number of problem arises in this structure firstly, the inputs can only change during the precharge phase and must be stable during the evaluate portion of the cycle. If this condition is not met, charge redistribution effects can corrupt the output node voltage.

For the delay analysis every transistor of the dynamic AND logic gate is model as resistor in series with an ideal switch. The propagation delay of the network excited by the step function is proportional to the time constant of the network. In this case time constant is the product of the resistor and load capacitor. Hence propagation delay for low to high transistor at 50% reach is

$t_{PHL} = \ln 2\ \tau = 0.69\ \tau = 0.69\ R_{onmos}\ CL$

where,

The on resistance of the NMOS and PMOS

$R_{onpmos} = 1/\mu CoxW/L(Vgs - Vt)p$,

$R_{onnmos} = 1/\mu CoxW/L\ (Vgs - Vt)n$

$t_{dp} = \sum_{i=1}^{N} Ci \sum_{i=1}^{L} Rj$

$t_{PHL} = 0.69(\ R1C3 + C2\ (R1+R2) + C1\ (\ R1+R2+R3)\ )$

if $R1=R2=R3 = R_N$

$t_{PHL} = 0.69R_N\ (C3 + 2C2 + 3C1)$

VI. Domino CMOS Logic :

A domino logic module consist of a pull down network (PDN), dynamically connected, followed by a static inverter as shown in fig . The non-inverting output of domino is represented by signal out while domino node is represented by P. The PDN is built exactly as that in complementary cmos. The domino module works in two phases - precharge and evaluation, where the signal clock controls the mode of operation In series connected dynamic structure consisting of several stages, after precharge the evaluation of each cascaded logic propagates the its evaluation to the next stage of dynamic logic. The structure is hence called domino CMOS logic. There are some other limitations associated with domino CMOS logic gates. The additional capacitance at each node of the series connected MOS logic makes speed slow and may cause charge redistribution which results in noisy output. During precharge phase, domino node P is charged to VDD by PMOS transistor MOS1. The NMOS transistor MOS1 is off during this phase. During evaluation phase, transistor mp1 is off while mn1 is in on state. If the input values are such that PDN conducts, node X discharges, otherwise it will hold the precharge value i.e. VDD.

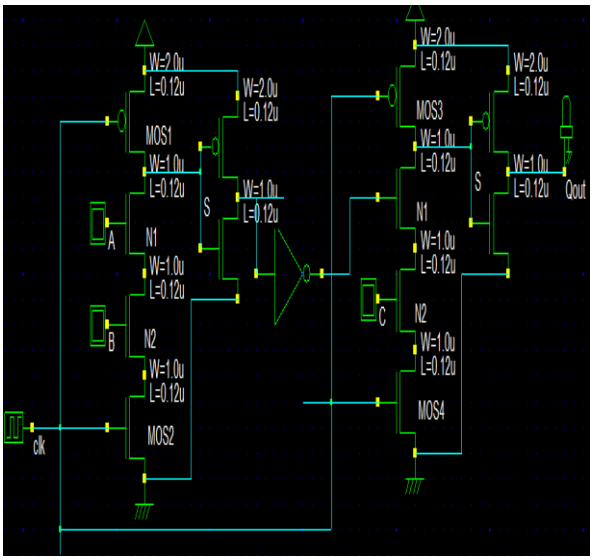

Fig 3: Domino CMOS Logic.

VII. Conclusion:

Dynamic CMOS logic circuits are widely employed in high-performance VLSI chips in pursuing very high system performance. However, dynamic CMOS gates are inherently less resistant to noises than static CMOS gates. With the increasing stringent noise requirement due to aggressive technology scaling, the noise tolerance of dynamic circuits has to be first improved for the overall reliable operation of VLSI chips designed using deep submicron process technology.

References:

[1] Smita Singhal, Anu Mehra, Upendra Tripathi "Power Reduction in Domino Logic using clock gating in 16nm CMOS Technology" 2019 9th International onference on Signal Processing and Integrated Network.

[2] Gaetano Palumbo,Melita Pennisi,and Massimo Alioto "A Simple Circuit Approach to Reduce Delay Variations in Domino Logic Gates" IEEE Transactions On Circuits And Systems—I: Regular Papers, Vol. 59, No. 10, October 2012

[3] Massimo Alioto, Gaetano Palumbo,and Melita Pennisi " Understanding the Effect of Process Variations on the Delay

of Static and Domino Logic" IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 18, No. 5, May 2010

[4] Kumar Dynamic CMOS Susceptible to Process Variations" IEEE Transactions On Semiconductor Manufacturing, Vol. 25, No. 2, May 2012 pp no. 255-265.Yelamarthi, and Chien-In Henry Chen "Timing Optimization and Noise Tolerance for Dynamic CMOS Susceptible to Process Variations" IEEE Transactions On Semiconductor Manufacturing, Vol. 25, No. 2, May 2012 pp no. 255-265.